FACULTY DEVELOPMENT PROGRAM

On

"Chip Design- A Fundamental Course"

27th to 31st Jan 2025

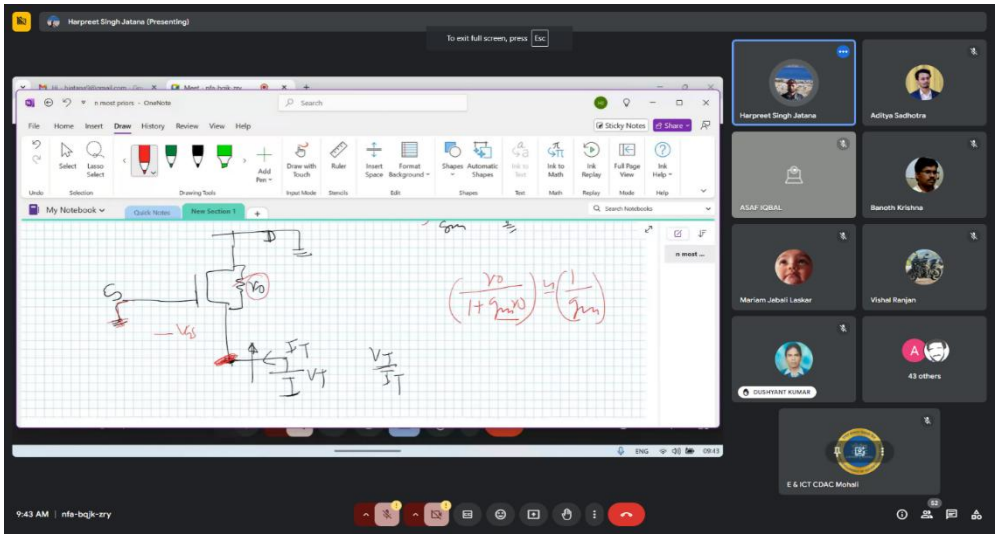
(Jointly organized by NIT Jalandhar and CDAC Mohali)

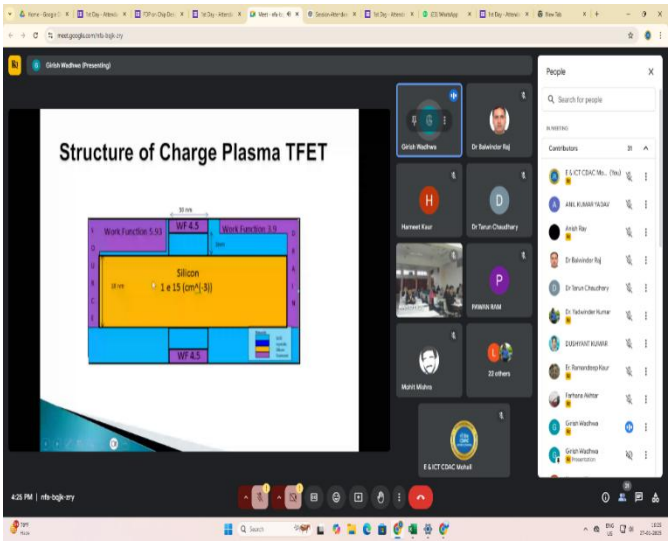
27th-January -2025(DAY-1)

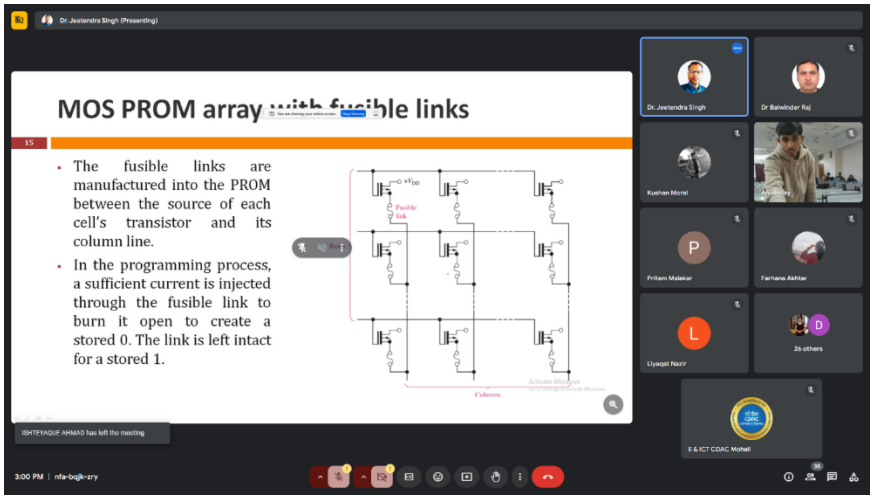
In this FDP experts from IITs, NITs and industries presented various lectures in the domain of chip design. Dr. Balwinder Raj and Dr. Tarun Chaudhary from NIT Jalandhar, along with experts from C-DAC Mohali and Assam University, Silchar, conducted practical sessions at their respective institutions on "Inverter Designing using Cadence Virtuoso." Participants learned to design a basic CMOS inverter through schematic capture, layout design, and simulation using this industry-standard tool. The sessions also covered transistor sizing, power consumption analysis, and performance optimization. These hands-on activities provided a strong foundation in VLSI design and enhanced participants' skills in digital circuit simulation.

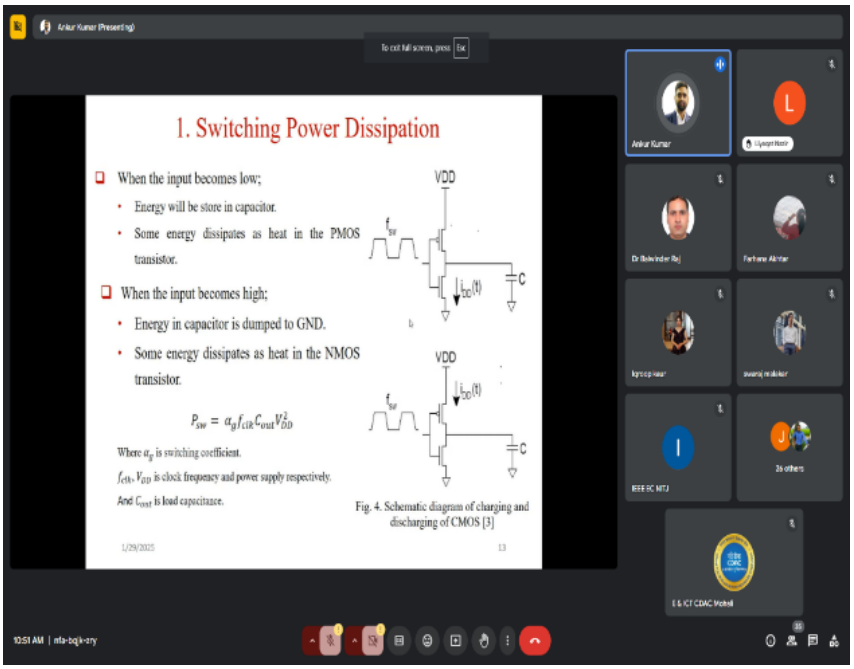
Coordinators from NIT Jalandhar, along with experts from C-DAC Mohali and Assam University, Silchar, also conducted practical sessions at their respective institutions on "Op-Amp Design using Cadence." Participants gained hands-on experience in designing operational amplifiers through schematic capture, transistor-level design, layout creation, and simulation. The session provided valuable insights into analog circuit design using the Cadence design suite. It helped students build essential skills in analog IC design and analysis with industry-standard tools.

Experts conducted practical sessions on Cadence Virtuoso, focusing on its application in VLSI design. Participants gained hands-on experience in schematic capture, layout creation, and circuit simulation using this industry-standard tool. The sessions covered key concepts like transistor sizing, design rules, and performance analysis, with guidance on optimizing and verifying circuit functionality. These activities equipped students with essential skills for real-world VLSI design and deepened their understanding of the semiconductor design process.


Harpreet Singh Jatana (Presenting)
To exit full screen, press Esc
Harpreet Singh Jatana
Aditya Sadhotra
ASAF IQBAL
Banoth Krishna
Mariam Jebali Lasker
Vishal Ranjan
DUSHYANT KUMAR
43 others
E & ICT CDAC Mohali
9:43 AM | nfa-bqjk-zry


Girish Wadhwa (Presenting)
Structure of Charge Plasma TFET
Work Function 5.93
WF 4.5
Work Function 3.5
Silicon
1 e 15 (cm^-3))
WF 4.5
People
Contributors
E & ICT CDAC Mohali
4:25 PM | nfa-bqjk-zry


Dr. Jeetendra Singh (Presenting)
MOS PROM array with fusible links
15
The fusible links are manufactured into the PROM between the source of each cell's transistor and its column line.
In the programming process, a sufficient current is injected through the fusible link to burn it open to create a stored 0. The link is left intact for a stored 1.
Fusible link
Columns
ISHTFYAQUF AHMAD has left the meeting
Dr. Jeetendra Singh
Dr Balwinder Raj
Kushan Monal
Pritam Malaker
Farhana Akhtar
Liyaqat Nazir
26 others
E & ICT CDAC Mohali
3:00 PM | nfa-bqjk-zry

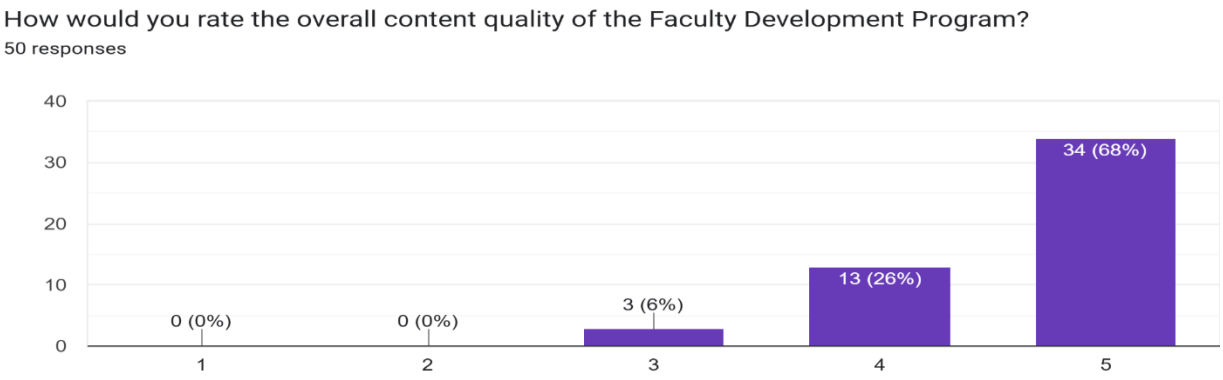


Group Discussion and Q&A

The session concluded with an evaluation exam, highlighting the significance of precision and optimization in chip design for modern electronics.

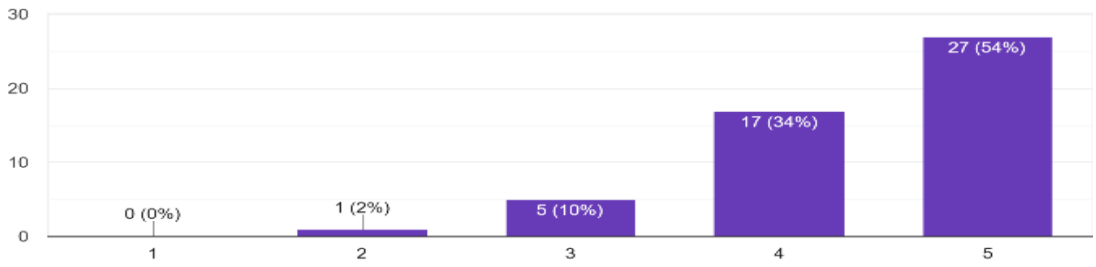
Reflection & Feedback session / Certificate Distribution

During the closing ceremony, participation certificates were distributed to all candidates. Attendees shared their experiences and insights, fostering community and collaboration. The session also served as a networking opportunity, connecting participants with experts and peers. The ceremony concluded with appreciation, emphasizing the continued exchange of ideas beyond the program.



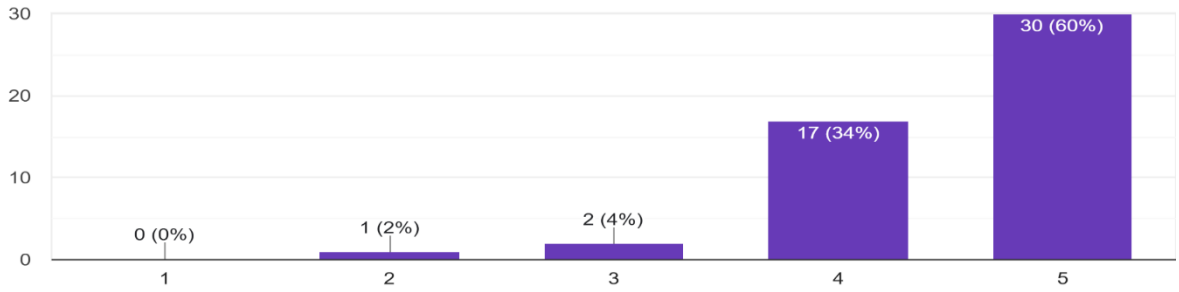
How would you rate the effectiveness of the hands-on sessions?

50 responses



How satisfied were you with the opportunities for networking and collaboration during the program?

50 responses



How satisfied were you with the quality of the speakers and their ability to engage the audience?

50 responses